

IN THE CLAIMS

Please amend the claims as follows:

Claims 1-4 (Canceled).

Claim 5 (Currently Amended): The semiconductor device comprising:

a semiconductor substrate;

an isolation insulating film selectively located in a surface of said semiconductor substrate; and

first and second transistors located respectively on first and second active regions which are defined by and in direct contact with said isolation insulating film,

said first transistor having a first gate insulating film of a first thickness which is selectively located on said first active region,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a recessed portion in an edge portion on the side of said first active region,

said recessed portion being located around said first active region,

a depth of said recessed portion is defined as a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm.

Claim 6 (Original): The semiconductor device according to claim 5, wherein  
said isolation insulating film has another recessed portion shallower than said  
recessed portion located around said first active region, in an edge portion on the side of said  
second active region,  
said shallower recessed portion is located around said second active region.

Claim 7 (Currently Amended): A semiconductor device comprising:  
a semiconductor substrate;  
an isolation insulating film selectively located in a surface of said semiconductor  
substrate; and  
a first transistor located on a first active region defined by and in direct contact with  
said isolation insulating film,  
said first transistor having a first gate insulating film of a first thickness which is  
selectively located on said first active region,  
said isolation insulating film having a first recessed portion in an edge portion on the  
side of said first active region, said first recessed portion being located around said first active  
region,  
a depth of said first recessed portion being defined as a vertical height between a main  
surface of said first active region and a deepest part of said first recessed portion and being  
not less than 10 nm.

Claim 8 (Original): The semiconductor device according to claim 7, further comprising:

a second transistor located on a second active region which is defined by said isolation insulating film as being different from said first active region in the surface of said semiconductor substrate,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a second recessed portion in an edge portion on the side of said second active region, said second recessed portion being located around said second active region,

a depth of said second recessed portion being defined as a vertical height between a main surface of said second active region and a deepest part of said second recessed portion and being not less than 10 nm.

Claim 9 (Original): The semiconductor device according to claim 7, further comprising:

a second transistor located on a second active region which is defined by said isolation insulating film as being different from said first active region in the surface of said semiconductor substrate,

said second transistor having a second gate insulating film of a second thickness which is selectively located on said second active region,

said first thickness being greater than said second thickness,

said isolation insulating film having a second recessed portion in an edge portion on the side of said second active region, said second recessed portion being located around said second active region.

Claim 10 (Canceled).

Claim 11 (Original): The semiconductor device according to claim 7, wherein said first transistor includes a transistor forming an input/output circuit, and said second transistor includes a transistor forming an analog circuit.

Claim 12 (Original): The semiconductor device according to claim 6, wherein said first transistor includes a transistor forming an input/output circuit, and said second transistor includes a transistor forming an analog circuit.

Claim 13 (Original): The semiconductor device according to claim 9, wherein said first transistor includes a transistor forming an input/output circuit, and said second transistor includes a transistor forming an analog circuit.